21154AC/BC and 21154AE/BE Differences

Application Note

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Contents

Tables

1.0 Introduction

This document describes the differences between the 21154AC when compared to the 21154AE and the 21154BC when compared to the 21154BE. The 21154AC/BC PCI-to-PCI Bridge integrated circuits were legacy custom designs produced in the Digital Equipment Corporation 0.5 micron CMOS technology. The 21154AE/BE replace the 21154AC/BC. The 21154AE/BE integrated circuits are ASIC designs using an Intel® 0.35 micron CMOS process and associated cell library.

The 21154AE and the 21154BE represent complete re-layouts of the original products. The pinouts are the same with one exception to accommodate the power management features. See Table 1 for a detailed description.

2.0 Stepping Differences

Table 1 summarizes circuit design changes between the 21154AC/BC and the 21154AE/BE.

Table 1. Circuit Design Changes

Item	21154AC	21154BC	21154AE	21154BE	Comment
Vendor ID	1011h	1011h	8086h	8086h	Change Vendor ID from Digital to Intel.
Device ID	0026h	0026h	B154h	B154h	Change to Intel format.
Revision ID	05h	05h	00h	00h	Reset Revision ID to 0 due to the Device ID change.
Logo	Intel	Intel	Intel	Intel	Incorporate into the physical layout of this design.
Power Management Enable Support	PME# support indication not enabled. Pin D11 is V_{DD}	PME# support indication not enabled. Pin D11 is V_{DD}	PME# support indication enabled. Pin D11 is PMEENA_L	PME# support indication enabled. Pin D11 is PMEENA_L	PMC bits [31:27] offset DEh are set as follows: When PMEENA_L is: • Asserted bits 31:27 offset DEh are set to logic “1”. • Deasserted the bits are set to logic “0”.
Marking	Intel® 21154AC DC1113B	Intel® 21154BC DC1113B	Intel® FW21154AE	Intel® FW21154BE	

Note: All hexadecimal numbers within the table are followed with a lowercase h.

3.0 Additional Differences

The following differences also exist for the 21154AE/BE versions:

- Viewing from the top of the 21154AE/BE package (marking side), the Pin 1 designator appears in the lower left hand corner of the package. The Pin 1 designator for previous revisions was in the upper left hand corner of the package.

- The 21154AE/BE has new ESD circuits. The qualification requirements for FLQ is 2000V minimum for HBM and 1000V minimum robustness for CDM. The 21154AE/BE meet the FLQ requirements with margin. For more information about these requirements, see the *Intel® (P854.6) PCI-to-PCI Bridge Customer Full Qualification Report, 01.27.01, Rev. 01*.
- The power sequencing scheme is different for the 21154AE/BE. A 50 to 100 ohm poly resistor was added in series with Vccref (internal circuit bias). The change allows the pads to handle 3.3- or 5-volt supplies powered up in any sequence.
- The PMEENA_L pin was changed to indicate that devices on the secondary side of the bridge do not support the PME# pin. It is up to the software then to scan the device to actually determine PME# pin support. This is described in Table 2 that follows:

Table 2. Power Management Capability Changes

Description	Value
Pin Number	D11
Previous Name	Vdd
Previous Function	Power Input
New Name	Pmeena_l
Function	Input
Operation	This can be tied to either Vdd or Vss (ground). This effects the value of bits [31:27], PME_SUP, of the Power Management Register (dword address DCh, offset DEh).
Vdd	These 5 bits should read a 00000[a], as in the old part values.
Vss	These 5 bits should read as 11111.

a. 00000 indicates that the device behind the bridge does not support PME#.

4.0 Errata

1. Tval Timing Issues When Running at 66 MHz for All PCI Signals (Both Bused and Control) on the 21154BC and 21554BE.

Problem: This problem exists for parts with REV_ID 5 and REV_ID 0.

Two worst-case slow conditions exist. The 21154BC and 21154BE were tested under two different sets of worst-case slow conditions.

Table 3. Definition of Worst-case Slow Conditions

Worst-Case Slow	T_{test} [T_j] (^oC)	Process Variation (Intel Defined)	V_{dd} (V)
Condition 1	85	S - slow	3.0
Condition 2	108	SS - very slow	3.0

Table 4. Comparison of the 21154BC and the 21154BE Performance

Product	Worst-case Slow Condition	Tval V_V (ns)	Tval Z_V (ns)
21154BC	1	6.5	8.0
21154BC	2	No data	No data
21154BE	1	6.5	6.5
21154BE	2	8.0	8.0

Implication: This miss for Tval on PCI control signals may reduce total flight time (Tprop) when running at 66 MHz. The 21154BE meets or exceeds the 21154BC performance under the worst-case slow conditions.

Workaround: There are no workarounds for this erratum.

Note: Refer to the *21154 PCI-to-PCI Bridge Specification Update* Errata table for current errata. All errata listed are fixed in the 21154AE/BE version except for Errata #1, #2, and #7.